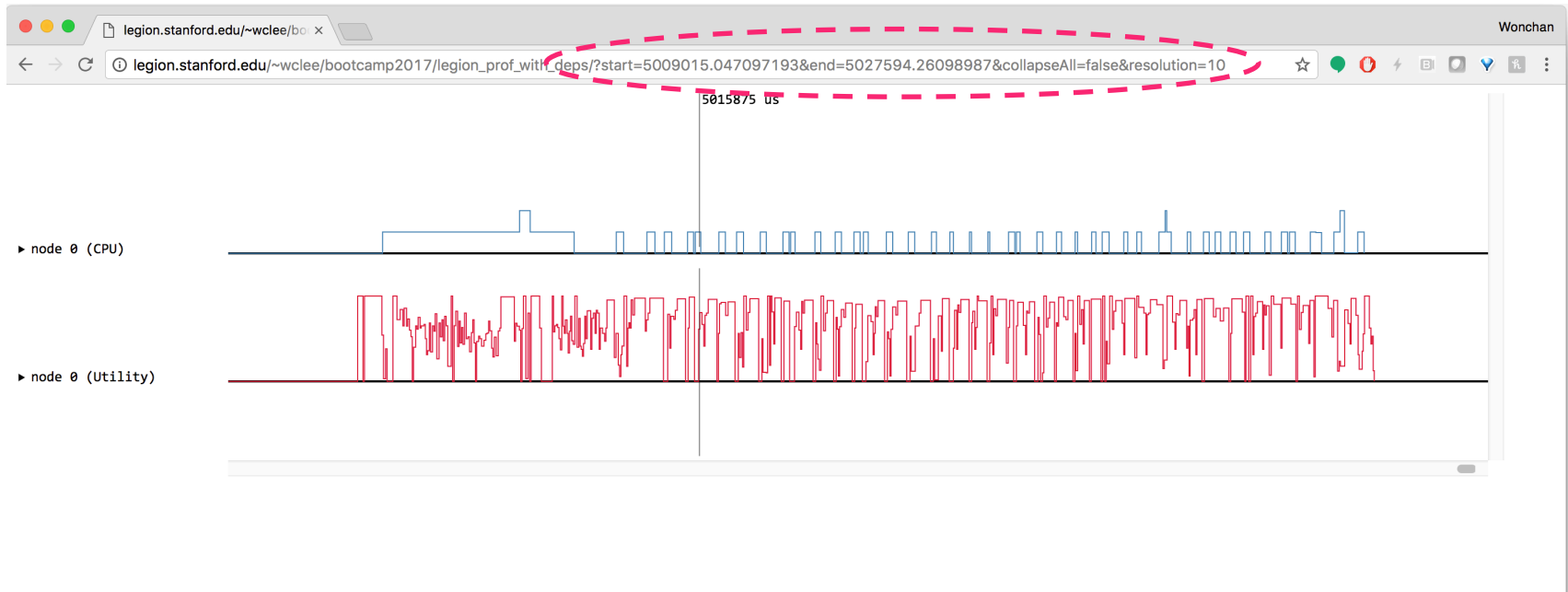


# Features in Legion Prof

Wonchan Lee

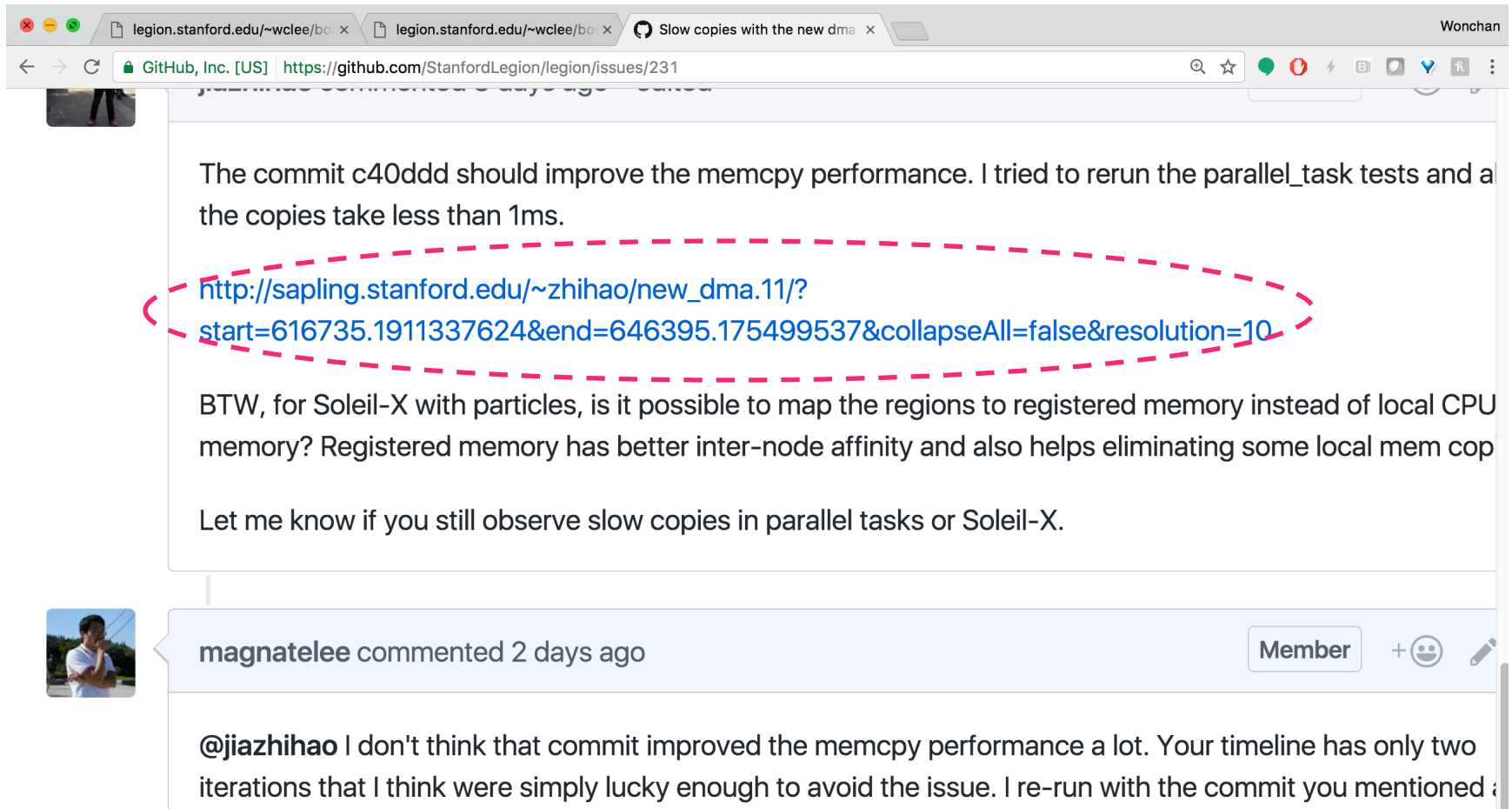
# URL String

- Remembers which time period the viewer was showing



# URL String

- Useful to share selections of interest in timelines



The screenshot shows a web browser window with the URL <https://github.com/StanfordLegion/legion/issues/231>. The page displays a GitHub issue discussion. The main comment, by user 'magnatelee', discusses a commit 'c40ddd' that improves memcpy performance. A red dashed oval highlights a URL string: [http://sapling.stanford.edu/~zhihao/new\\_dma.11/?start=616735.1911337624&end=646395.175499537&collapseAll=false&resolution=10](http://sapling.stanford.edu/~zhihao/new_dma.11/?start=616735.1911337624&end=646395.175499537&collapseAll=false&resolution=10). Below this, the user asks a question about mapping regions to registered memory for Soleil-X. A reply from user '@jjazhihao' is partially visible at the bottom.

The commit c40ddd should improve the memcpy performance. I tried to rerun the parallel\_task tests and the copies take less than 1ms.

[http://sapling.stanford.edu/~zhihao/new\\_dma.11/?start=616735.1911337624&end=646395.175499537&collapseAll=false&resolution=10](http://sapling.stanford.edu/~zhihao/new_dma.11/?start=616735.1911337624&end=646395.175499537&collapseAll=false&resolution=10)

BTW, for Soleil-X with particles, is it possible to map the regions to registered memory instead of local CPU memory? Registered memory has better inter-node affinity and also helps eliminating some local mem cop

Let me know if you still observe slow copies in parallel tasks or Soleil-X.

magnatelee commented 2 days ago

@jjazhihao I don't think that commit improved the memcpy performance a lot. Your timeline has only two iterations that I think were simply lucky enough to avoid the issue. I re-run with the commit you mentioned

# Zoom

- Keyboard shortcuts
  - **Ctrl-Alt -** or **1** – Zoom out (y-axis)
  - **Ctrl-Alt +** or **2** – Zoom in (y-axis)
  - **Ctrl -** or **3** – Zoom out (x-axis)
  - **Ctrl +** or **4** – Zoom in (x-axis)
  - **Ctrl 0** or **0** – Reset zoom (x-axis)
- Drag-select to zoom in for a particular range
  - Will show only the time span if CMD is pressed
  - Can be undone with **U**

# Search

- Find matches on the names of tasks with regex
- Keyboard shortcuts
  - **S** – Start a new search
  - **T** – Toggle search
  - **N** – Switch to the next search
  - **P** – Switch to the previous search
  - **H** – Show the search history
  - **C** – Clear the search history
- Search query is also encoded in URL string

# Dependency Tracking

- Show dependencies of each operation in the timeline
- Require both Legion Prof and Legion Spy outputs
  - Legion Spy might introduce some overhead
- Critical path analysis will be coming up shortly!

# Mapper DSL

Wonchan Lee

# Writing Mappers is Tedious

- Verbosity in the C++ API
- Differences between Regent and Legion
  - Region names vs. region requirements
  - Field names vs. field IDs
  - Compiler optimizations that generate non-user tasks

# Writing Mappers is Tedious

- Verbosity in the C++ API
- Differences between Regent and Legion
  - Region names vs. region requirements
  - Field names vs. field IDs
  - Compiler optimizations that generate non-user tasks
- Mapper is not part of the Regent language

```
local circuit_cc = root_dir .. "circuit_mapper.cc"  
local circuit_so = root_dir .. "libcircuit.so"  
os.execute("c++ -O2 -Wall -Werror -shared -fPIC " ..  
           circuit_cc .. " -o " .. circuit_so)  
terralib.linklibrary(circuit_so)  
local ccircuit = terralib.includec("circuit_mapper.h")
```

# Bishop: A High-level Mapper DSL

- CSS-like syntax

```
<html>
  <body>
    <p id="block1">Bigger</p>

    <p id="block2">Smaller</p>
  </body>
</html>
```

HTML

```
p#block1 {
  font-size: 30pt;
}

p#block2 {
  font-size: 10pt;
}
```

CSS

# Bishop: A High-level Mapper DSL

- CSS-like syntax

```
task child(r : region(...))
  ...
end

task parent(r : region(...))
  child(r)
end
```

Regent

```
task#parent {
  target-kind: x86;
}

task#child {
  target-kind: cuda;
}

task#child region#r {
  target-kind: fbmem;
}
```

Bishop

# Bishop: A High-level Mapper DSL

- CSS-like syntax

```
task child(r : region(...))  
  ...  
end  
  
task parent(r : region(...))  
  child(r)  
end
```

Regent

```
task#parent {  
  target-kind: x86;  
}  
  
task#child {  
  target-kind: cuda;  
}  
  
task#child region#r {  
  target-kind: fbmem;  
}
```

Bishop

- Keep the separation between description and execution

# Circuit Example

```
$CPUs = processors[isa=x86]
$GPUs = processors[isa=cuda]
$HAS_GPU = $GPUs.size > 0

-- Mapping policies for Tasks

task {
  target : $CPUs;
}

task#calculate_new_currents[index=$i] {
  target : $HAS_GPU ? $GPUs[$i % $GPUs.size] : $CPUs[$i % $CPUs.size];
}

-- Mapping policies for Regions

task[isa=x86 and target=$p] region {
  target : $p.memories[kind=systemem];
}

task[isa=cuda and target=$p] region {
  target : $p.memories[kind=fbmem];
}

task#calculate_new_currents[isa=cuda and target=$p] region#rsn {
  target : $p.memories[kind=zcmem];
}

task#calculate_new_currents[isa=cuda and target=$p] region#rgn {
  target : $p.memories[kind=zcmem];
}
```

- 
- The diagram illustrates a state transition graph for the circuit\_bishop problem. The graph consists of 21 states, labeled state 0 through state 20. State 0 is the root node, colored red, and is labeled "state 0". It transitions to state 1, labeled "state 1" and "current task: toplevel", via the "toplevel" edge. State 1 is a white oval. From state 1, there are three outgoing edges: "[isa=x86]" to state 9, "[isa=cuda]" to state 10, and "block\_task" to state 7. State 9 is a blue oval labeled "state 9" and "current task: toplevel", with the task description "task[isa=x86][target=\$p] region (circuit\_bishop.rg:39)". State 10 is a blue oval labeled "state 10" and "current task: toplevel", with the task description "task[isa=cuda][target=\$p] region (circuit\_bishop.rg:35)". State 7 is a white oval labeled "state 7" and "current task: block\_task". From state 9, there are three outgoing edges: "init\_piece" to state 4, "calculate\_new\_currents" to state 4, and "init\_pointers" to state 4. From state 10, there are three outgoing edges: "calculate\_new\_currents" to state 4, "distribute\_charge" to state 7, and "block\_task" to state 7. From state 7, there are two outgoing edges: "[isa=x86]" to state 13 and "[isa=cuda]" to state 20. State 4 is a blue oval labeled "state 4" and "current task: calculate\_new\_currents", with the task description "task#calculate\_new\_currents[index=\$i] (circuit\_bishop.rg:28)". From state 4, there are two outgoing edges: "[isa=x86]" to state 20 and "[isa=cuda]" to state 20. State 13 is a blue oval labeled "state 13" and "current task: block\_task", with the task description "task[isa=x86][target=\$p] region (circuit\_bishop.rg:39)". State 20 is a blue oval labeled "state 20" and "current task: calculate\_new\_currents", with the task description "task[isa=cuda][target=\$p] region (circuit\_bishop.rg:35)", "task#calculate\_new\_currents[index=\$i] (circuit\_bishop.rg:28)", "task#calculate\_new\_currents[isa=cuda][target=\$p] region#rsn (circuit\_bishop.rg:43)", and "task#calculate\_new\_currents[isa=cuda][target=\$p] region#rgn (circuit\_bishop.rg:47)". The graph shows a complex sequence of tasks and their parameters across different states, with some states having multiple outgoing edges and some having multiple task descriptions.

# Plan

- Make the language feature complete
  - Copy operations
  - Layout constraints for physical instances
  - Error handling
- Static analysis to generate mappers for Regent programs
- Optimize Regent task variants based on mapping policies